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ABSTRACT

Trombley, Gerald J., Transient Radiation Hardened CMOS Operational Amplifiers. (Under the direction of Dr. John J. Paulos.)

General strategies are developed for designing radiation hardened bulk and silicon on insulator (SOI) complementary metal oxide semiconductor (CMOS) operational amplifiers. Comparisons are made between each technology concerning photocurrent mechanisms and the inherent advantages of SOI CMOS. Methods are presented for analyzing circuit designs and minimizing the net photocurrent responses. Analysis is performed on standard operational amplifier circuits and subcircuits to demonstrate the usefulness of these methods.

Radiation hardening topics discussed include superior radiation hardened topologies, photocurrent compensation and its limitations, and methods to ensure a preferred direction of photocurrent response. Several operational amplifier subcircuits are compared for their hardness characteristics.

Folded cascode and three-stage operational amplifiers were fabricated on an SOI CMOS test chip supported by Texas Instruments, Incorporated. At the time of publication, the circuit operation was verified but radiation data were not yet available.

Transient Radiation Hardened

CMOS Operational Amplifiers

by

Gerald J. Trombley

A thesis submitted to the Graduate Faculty of
North Carolina State University
in partial fulfillment of the
requirements for the Degree of
Master of Science

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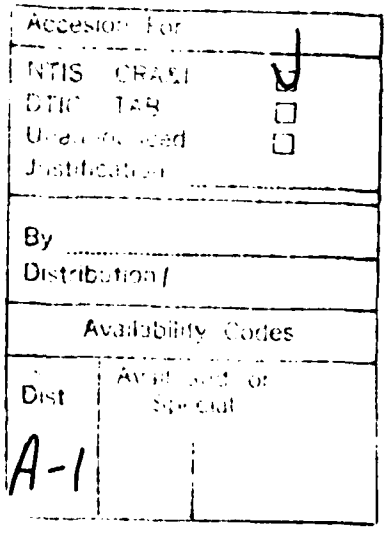
Most of all, I wish to thank my wife, Jessica, whose endless support has made this degree possible.



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CHAPTER 1: INTRODUCTION

1.1 RADIATION ENVIRONMENTS

Radiation effects are a critical concern for integrated circuits operating in space or nuclear weapons environments. Radiation effects in space environments arise primarily from relatively low levels of radiation exposure over extended periods of time. An example is the use of IC's in communication satellites which must operate reliably for many years. These long-term effects, called total dose effects, commonly cause shifts in device parameters that may degrade circuit performance and eventually render the circuit useless. Additional space environment effects include cosmic rays that can cause loss of data at isolated nodes in a dynamic or static memory.

In contrast, weapons environment radiation, also called transient radiation, generally involves short-term, high-intensity radiation exposure. Here system performance or functionality may be interrupted by the effects of a nearby nuclear detonation. These exposures cause generation of photocurrents within the integrated circuit device structures that occur with magnitudes in proportion

to the magnitude of the radiation transient. Systems in these environments may be expected to operate through the radiation transient or merely to recover quickly immediately following the radiation exposure.

1.2 MOTIVATION

Today, there is a growing need for radiation hardened analog circuits for on-chip applications. With denser fabrication processes and a growing use of high complexity, custom integrated circuits, radiation-hardened operational amplifiers are often needed on the same integrated circuit substrate as hardened digital circuits.

This thesis considers the design of operational amplifiers for transient radiation environments using CMOS (Complementary Metal Oxide Semiconductor) technology. First, an overview of photocurrent responses in bulk and silicon on insulator (SOI) CMOS technologies is presented. Next, methods for testing CMOS operational amplifiers for radiation hardness are discussed and several design strategies are developed. Finally, these implementation issues are demonstrated through the design of folded-cascode and three-stage amplifiers. These designs are included on a test chip which has been fabricated in an SOI CMOS process by Texas Instruments, Incorporated.

CHAPTER 2: BACKGROUND

2.1 MECHANISMS OF IONIZING RADIATION

Before strategies can be developed for radiation hardening of operational amplifiers, the basic radiation photocurrent mechanisms must be considered. In the following sections, simple one-dimensional diode photocurrent mechanisms will be discussed followed by three-dimensional photocurrent mechanisms for bulk CMOS and SOI CMOS technologies. An example of the transient radiation response of an operational amplifier circuit fabricated in a bulk CMOS technology is included to demonstrate the expected effects of radiation photocurrents.

2.1.1 ONE-DIMENSIONAL DIODE

Radiation exposure produces additional free carriers in silicon. The unit of radiation exposure is the rad, which is defined as the deposition of 100 ergs per gram of radiation energy into a material. In bulk silicon, approximately $4.2 \cdot 10^{13}$ electron-hole pairs/cm^3 are generated per rad [2]. These electron and hole carriers may contribute to photocurrents depending on their proximity to a pn

junction.

In 1963, Wirth and Rogers developed a model for a one-dimensional transient diode photocurrent as shown in Figure 2.1 [6]. The carriers that originate in the depletion region produce so called prompt photocurrents because these electrons and holes are swept almost instantaneously to the contacts by the electric field within the depletion region. Free holes travel in the direction of the field towards the n-region contact and free electrons travel in the opposite direction towards the p-region contact. Virtually all carriers in this region contribute to photocurrent since the electron and hole recombination lifetimes are much longer than the depletion region carrier transport times.

The carriers that originate within one diffusion length of the depletion region may cause diffusion photocurrents. These free carriers must diffuse to the edge of the depletion region before they are swept through the

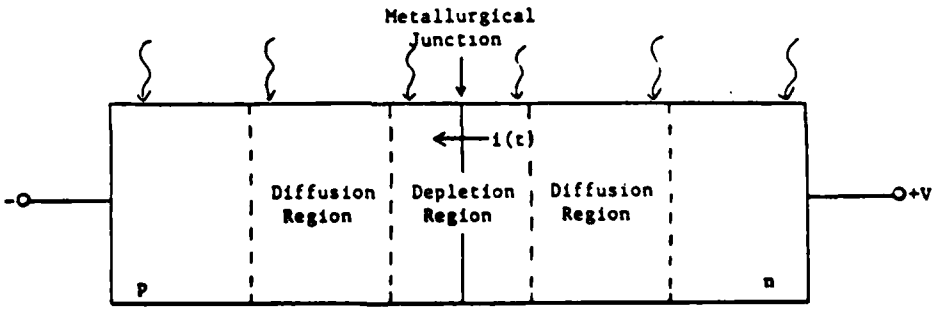

Figure 2.1: One-dimensional diode model, from Massengill [2]

depletion region. Diffusion photocurrents are delayed relative to the actual radiation transient since these carriers diffuse for up to one carrier lifetime before they reach the depletion region. Therefore, diffusion photocurrents occur up to approximately one carrier lifetime after the prompt photocurrent.

The magnitude of the prompt photocurrent is proportional to the volume of the pn junction depletion region. The width of the depletion region is dependent upon the bias voltage and the silicon junction doping levels. The depletion region width is approximated by the following equation,

$$W = \left[\frac{2\varepsilon V_o}{q} \left[\frac{1}{N_a} + \frac{1}{N_d} \right] \right]^{\frac{1}{2}} .$$

where

ε is the permitivity of silicon,

Vo is the reverse bias potential applied to the junction contacts,

q is the unit charge of an electron; 1.6E-19 C,

Na is the acceptor dopant concentration on p-side of junction, and

Nd is the donor dopant concentration on n-side of junction.

Higher prompt currents are expected for greater reverse bias voltages since higher reverse bias voltages yield larger depletion regions.

The magnitude and duration of diffusion photocurrents

is primarily dependent upon the diffusion lengths of the carriers and the surface area of the junction depletion region. Carrier diffusion lengths are determined by the following equation,

$$L = \sqrt{D\tau} \ ,$$

where

D is the diffusivity coefficient and

τ is the carrier recombination lifetime.

If the diffusion coefficient is considered constant, the diffusion length is proportional to the square root of the carrier recombination lifetime. Thus, the diffused photocurrent is a strong function of process variables in addition to the physical dimensions of the devices.

2.1.2 BULK CMOS

Figure 2.2 shows a partial cross section of a typical p-well CMOS process including the photocurrent collection volumes. The expected radiation photocurrents generated may be approximated using a three-dimensional photocurrent response model [2]. For each junction, the photocurrent model will include the photocurrent collection volume dimensions based on bias voltages, doping levels and diffusion lengths. These models must often allow for physical obstructions on the wafer that could limit the

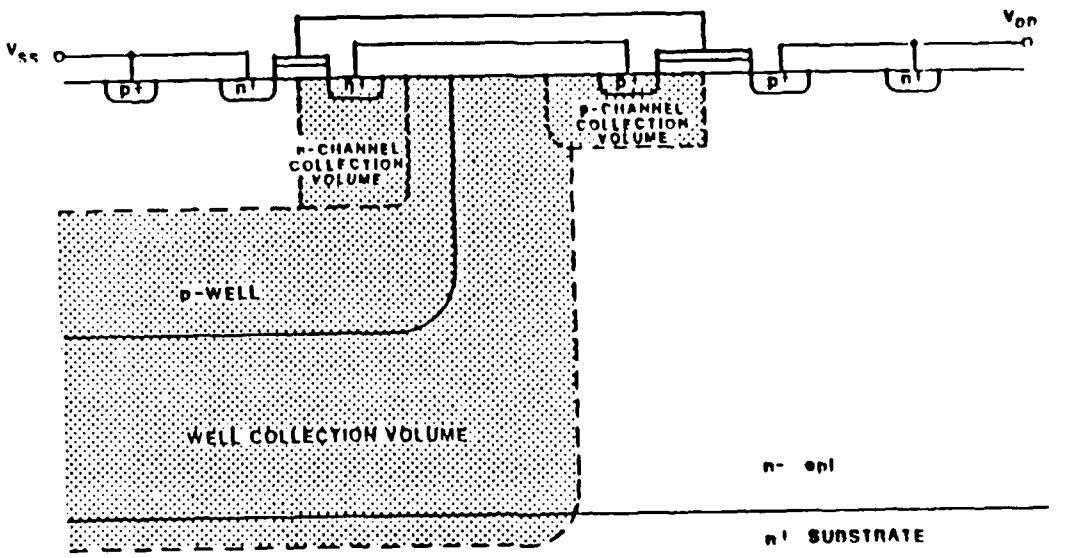

Figure 2.2: Typical p-well CMOS structure, from Massengill [2]

photocurrent collection volumes.

A higher junction reverse bias voltage generally causes an increase in the photocurrent collection volume. However, the photocurrent collection volumes may be limited by obstructions on the wafer such as an isolation trench or an adjacent junction. If this occurs, increases in reverse bias may not lead to the expected increase in prompt photocurrent, and diffused photocurrents may even decrease.

The photocurrent sources in CMOS technologies may either load the power supply directly, without affecting any circuit node, or they may load the power supply indirectly through a circuit node. Well-to-substrate photocurrent sources load the power supply directly since there is no physical connection to any circuit nodes. Generally

source-to-substrate or drain-to-substrate photocurrent sources and source-to-well or drain-to-well photocurrent sources apply photocurrents to internal circuit nodes. Due to the inherently large photocurrent collection volumes of well-to-substrate photocurrent sources, these photocurrents usually comprise most of the power supply drain during radiation transients in bulk CMOS technologies.

An additional consideration in radiation environments is bulk CMOS latchup. Figure 2.3 shows a drawing and schematic of the latchup structure. Notice that the complementary MOS transistors form a lateral pnpn structure that is modeled in the schematic as back to back connected npn and pnp transistors. In radiation environments, latchup may be caused by photocurrents either raising the base potential in the npn structure or lowering the base potential in the pnp structure past a critical level. When latchup occurs, the combined npn and pnp structures conduct and the attached MOS devices may burn out or cause a circuit malfunction. Generally, to unlatch the structure the power supply voltage must be removed and then reapplied. To avoid latchup, oxide trenches may be used to introduce isolation between adjacent devices. Alternatively, the interdevice spacings may be increased, which reduces circuit density.

Figure 2.4 shows a schematic of a p-well CMOS differential amplifier including photocurrent sources. There are two radiation photocurrent sources from the p-well to the

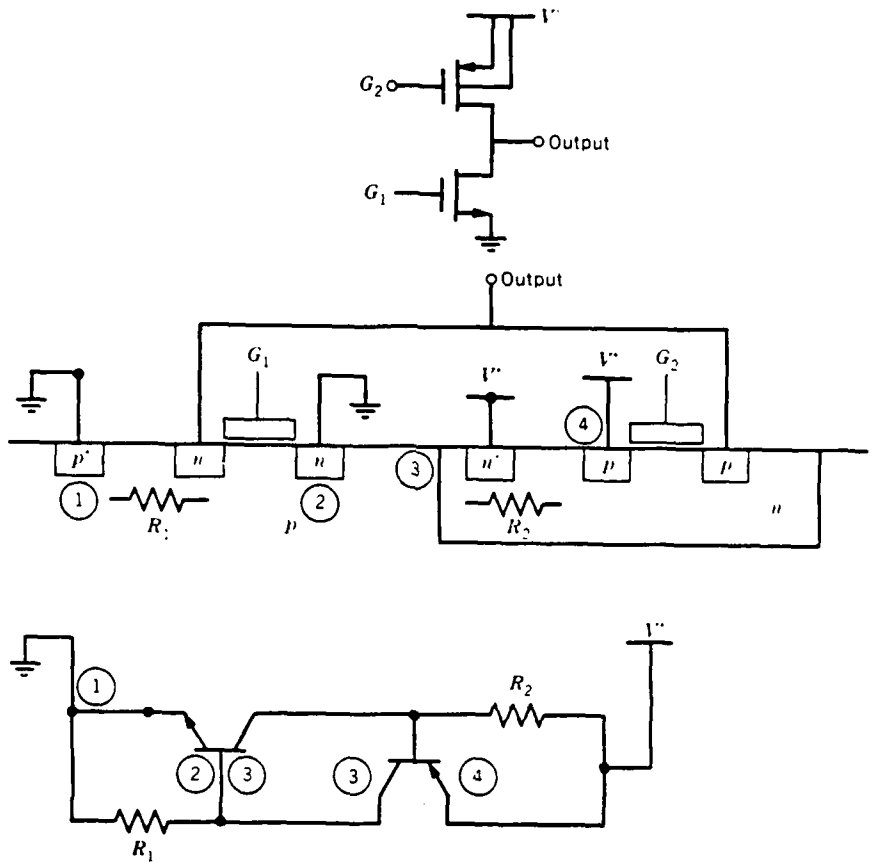

Figure 2.3: Crossectional view of a bulk CMOS structure illustrating the lateral pnpn structure, from Grey and Meyer [1]

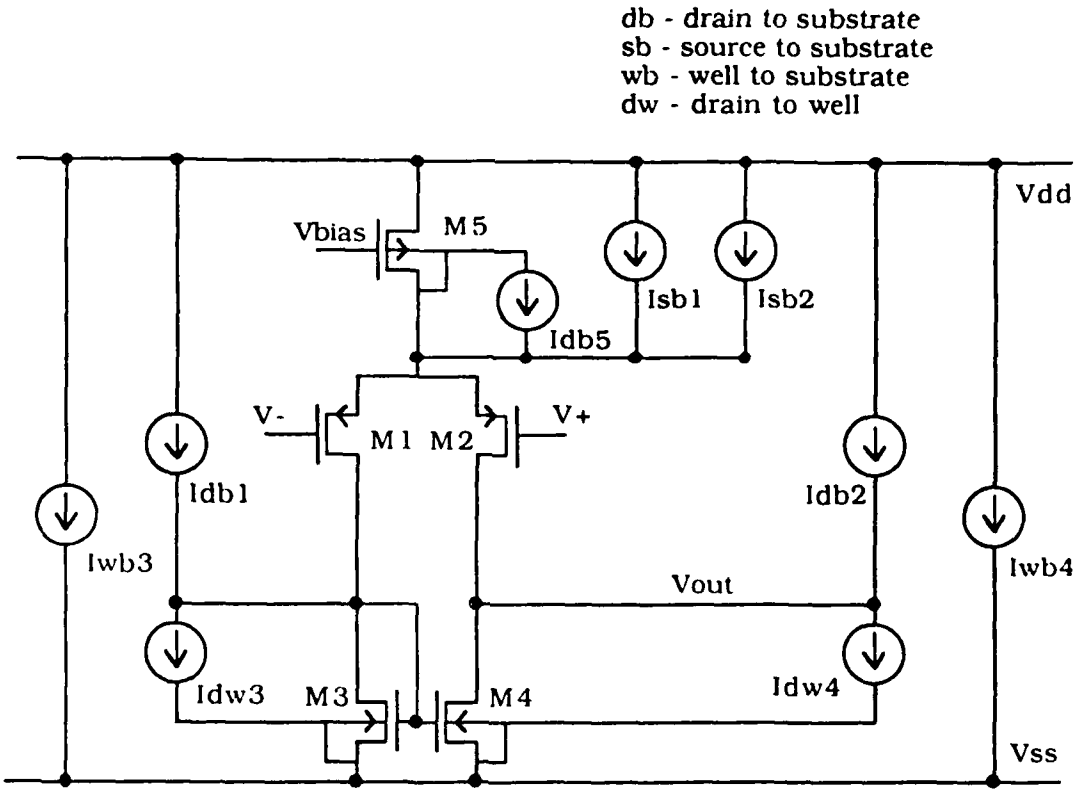

Figure 2.4: P-well differential amplifier with photocurrent sources

substrate, Iwb3 and Iwb4, associated with transistors M3 and M4, respectively. These photocurrent sources load the power supply directly without affecting any circuit node. The photocurrent sources Idb1 and Idw3, Idb2 and Idw4, and Isb1, Isb2 and Idb5, introduce photocurrents at the drains of M1, M2 and M5, respectively. These photocurrents may cause voltage perturbations at their respective nodes.

Given that the power supply voltages are not significantly affected by the radiation transient, the primary concern is to minimize the photocurrent response at

sensitive circuit nodes. For the differential amplifier in Figure 2.4, the greatest sensitivity to radiation induced photocurrents is at the drains of M1 and M2. The photocurrent source pairs are of opposite polarity at the drains of M1 and M2 because they are formed from complementary device types. A minimal net photocurrent response will occur at the output node if the photocurrent components are approximately equal. Therefore, proper matching of n-channel and p-channel transistor photocurrent collection volumes will minimize the net photocurrents generated at a node for bulk CMOS technologies.

2.1.3 SOI CMOS

In SOI CMOS, the primary photocurrent mechanism is a drain-to-source current generated in the thin transistor body layer. Figure 2.5 shows the cross section of an n-channel SOI transistor. Note that the only photocurrent path is from drain to source. In addition, the photocurrents generated for SOI are confined to the thin silicon layer (generally less than 1 micron) of the active area of the transistor. This significantly reduces the photocurrent response of each SOI device as compared with bulk CMOS technologies.

Floating-body effects with SOI CMOS devices may significantly affect their performance in radiation environments. The simulated Id vs. Vds curves for an SOI

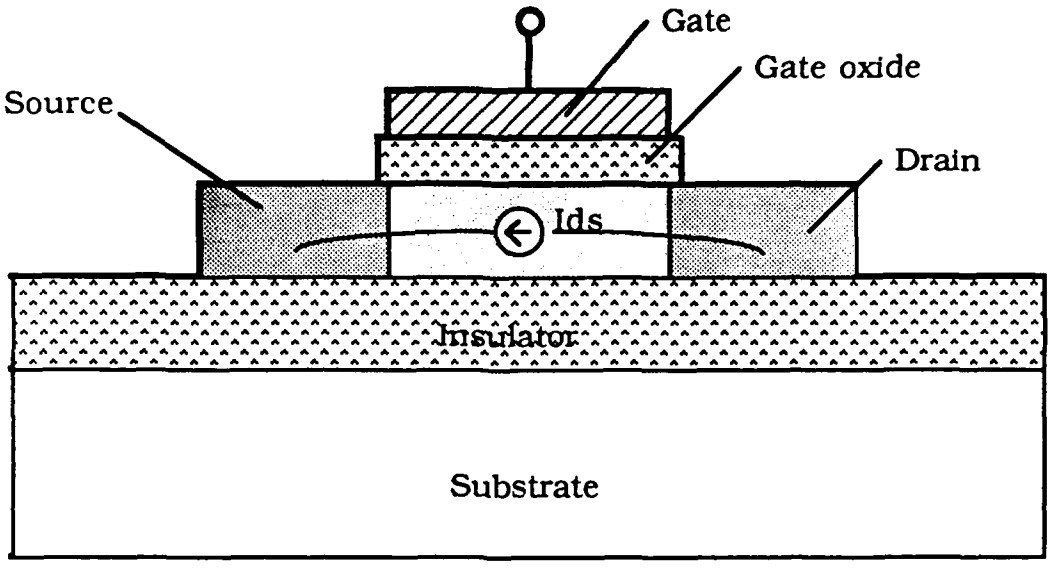

Figure 2.5: Cross section of n-channel SOI transistor with photocurrent source

floating-body transistor in Figure 2.6 shows the deterioration of the output conductance at moderate to high current levels. These "kinks" in the device curves are caused by an avalanche mechanism within the transistor body that generate additional mobile carriers [5]. A similar mechanism called the photocurrent multiplier effect may occur in SOI technologies which causes the apparent photocurrents across the drain-to-source to exceed the radiation-induced photocurrent due to electron-hole pair generation alone. This increased photocurrent may also be less predictable and controllable. A solution to the floating-body problem is to tie the source to the body during the fabrication process. Body-tied-to-source

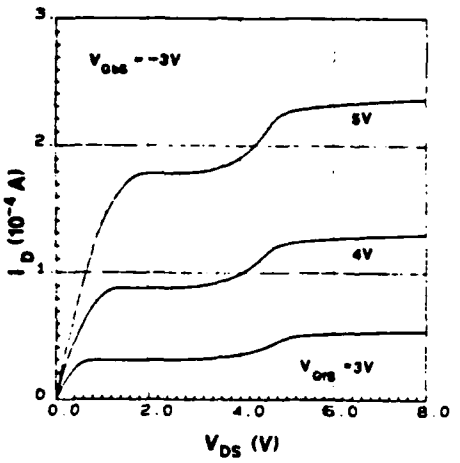

Figure 2.6: Simulated SOI CMOS Id(Vds,Vgs) characteristics showing floating body kink effect, from Veeraraghavan, Fossom, and Eisenstadt [5]

configurations are used in Chapter 5 with Texas Instruments' SOI CMOS process.

In body-tied-to-source devices, photocurrents may be approximated by assuming that the total body area is depleted and that all electron-hole pairs generated within the body contribute to a prompt photocurrent. Figure 2.7 shows a schematic of a differential amplifier in SOI CMOS with photocurrent sources included. Notice that each device has a drain-to-source photocurrent source only. As in the bulk CMOS example, the drains of M1 and M2 are the nodes that are the most sensitive to radiation photocurrents. Photocurrent sources Ids1 and Ids3 apply and remove currents at the drain of M1, and photocurrents Ids2 and Ids4 apply and remove currents at the drain of M2.

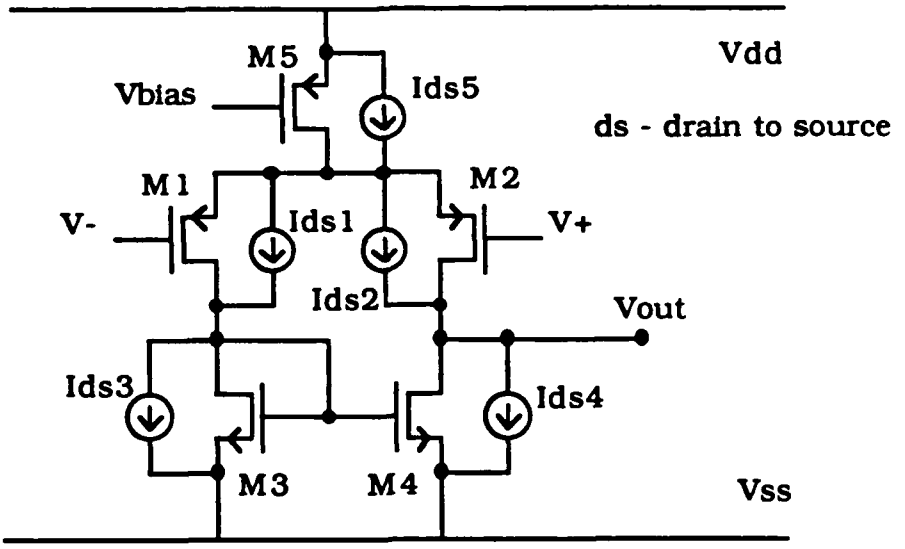

Figure 2.7: SOI CMOS differential amplifier with photocurrent sources

Therefore, if photocurrent pairs Ids1 and Ids3 and Ids2 and Ids4 are approximately equal, a minimal photocurrent response will be observed.

2.2 PHOTOCURRENT MODELING UNCERTAINTIES

If photocurrent matching strategies are to be used to limit the photocurrent response at a node, accurate photocurrent models are needed. Bulk CMOS has a number of physical properties that significantly impact photocurrent predictability. Notice that for the p-well CMOS process shown in Figure 2.2, the depth of collection is limited by the p-well depth in the n-channel case and by the substrate thickness in the p-channel case. Also, in the n-channel case, the depletion regions of the source-to-p-well and

drain-to-p-well junctions and the p-well-to-substrate junctions are competing for diffused electrons and holes while in the p-channel case, no such competition is present. As yet another source of photocurrent uncertainty, lateral collection at sources and drains of n-channel and p-channel devices is limited by adjacent source and drain structures and by the substrate-to-p-well interfaces which extend to the surface. Finally, uncertainties in carrier lifetimes limit the accuracy of diffused photocurrent collection volumes. These various characteristics suggest large uncertainties in photocurrent production for bulk CMOS circuits.

A number of steps can be taken to improve radiation photocurrent predictability for bulk CMOS technologies. Using larger spacings between devices and between devices and p-well-to-substrate interfaces would help to avoid competition for diffused photocurrent carriers but this strategy generally decreases circuit densities. Also, doping the substrate with lifetime killers such as gold will significantly reduce the diffused radiation photocurrent component and may improve the carrier lifetime predictability. In general, any process or fabrication technique that improves the photocurrent collection volume predictability may be a worthy consideration for improving the radiation hardness.

2.3 OPERATIONAL AMPLIFIER TRANSIENT RADIATION RESPONSE

Figure 2.8 shows the transient radiation response of a three-stage operational amplifier fabricated in a bulk CMOS technology. Flash X-ray is used as the radiation source with a dose rate calibrated to $3 \cdot 10^7$ rads(Si)/sec. Figure 2.9 shows the simulated output response of this circuit. Here the photocurrents responses are separated into three groups, photocurrents along the signal path, within the bias circuit, and at the output. Due to the nonlinearity of the amplifier response to the bias circuit photocurrents, the overall responses is not a simple superposition of the separate photocurrent responses [3].

As we can see, the output response of any operational amplifier is determined by a complex combination of

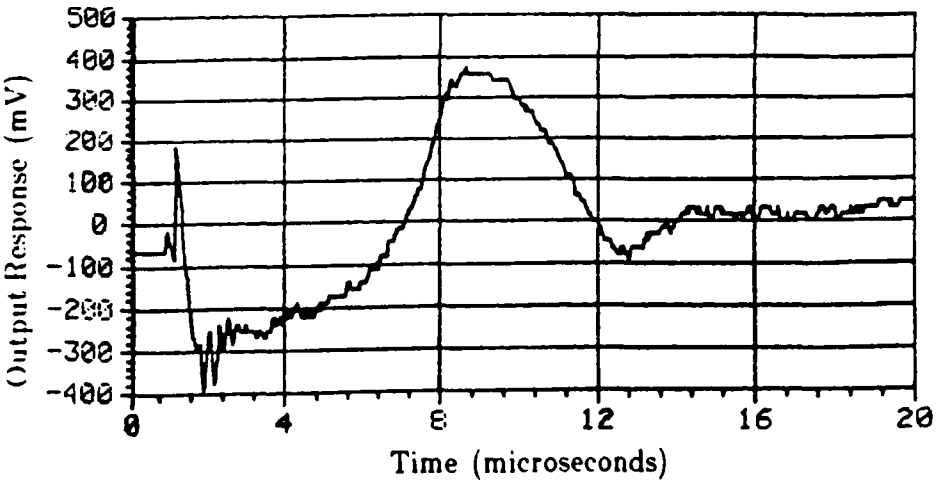

Figure 2.8: Three-stage operational amplifier transient radiation response, from Paulos and Bishop [3]

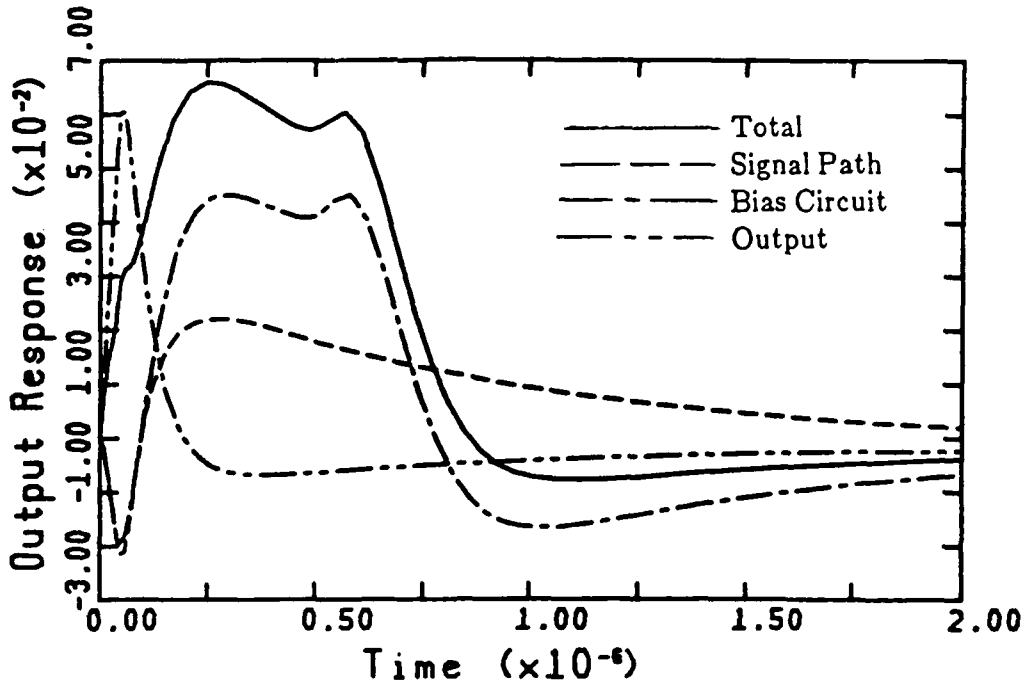

Figure 2.9: Simulated operational amplifier transient radiation response, from Paulos and Bishop [3]

factors. These factors include the radiation dose rate and duration, the operational amplifier configuration and load, the stability of the power supply during the radiation transient, and the internal response of the operational amplifier itself. Therefore it is important to identify and control each factor that contributes to a photocurrent response. In the following chapters, the primary strategy followed is to minimize the photocurrent response at each circuit node individually by using straight forward compensation techniques. However, before these compensation techniques are discussed, analysis techniques will be developed that can be used to identify sensitive nodes and

to estimate the operational amplifier circuit response.

CHAPTER 3: ANALYTICAL TESTING

3.1 INTRODUCTION

This chapter will cover some recommended methodologies for testing operational amplifier topologies and design specifications. Analysis falls into two general categories, steady-state analysis and transient analysis, which relate to steady-state and transient radiation environments, respectively. These methods are useful for demonstrating the advantages and disadvantages of various operational amplifier topologies and radiation hardening strategies.

3.2 PHOTOCURRENT MODELS

Whether bulk or SOI CMOS technologies are to be used, many circuit design consideration are common to both. In general, CMOS operational amplifiers may be modeled as standard operational amplifier circuits with the addition of net photocurrent sources applied at the circuit nodes. This method aids in the discussion of topology issues for bulk and SOI CMOS technologies simultaneously. However, in some applications net photocurrent source models may be undesirable since the actual supply currents are not

simulated during the transient.

3.3 STEADY-STATE ANALYSIS

Steady-state analysis can be used to simulate radiation transients of relatively long duration (microseconds to milliseconds). An example that may be encountered in defense applications is a moderate-level energy beam that is designed to cause a temporary or permanent circuit malfunction in an observation satellite or defense system. A malfunction may be caused by temporarily upsetting the operating performance of the circuit or by permanent device damage due to prolonged excess power dissipation.

Steady-state radiation environments allow for an operational amplifier's closed-loop response to compensate for the radiation photocurrents. In cases where the radiation exceeds a critical level, the operational amplifier may no longer have the capability to compensate, through feedback, for the photocurrents present. In either case, the expected steady-state response for a given circuit may be determined through steady-state analysis or simulation. In this paper, all simulations are performed using the SPICE circuit simulation program.

Steady-state analysis is performed on the unity-gain configured, two-stage operational amplifier shown in Figure 3.1. The net photocurrent source levels listed in Table 3.1 are typical steady-state photocurrent responses per unit

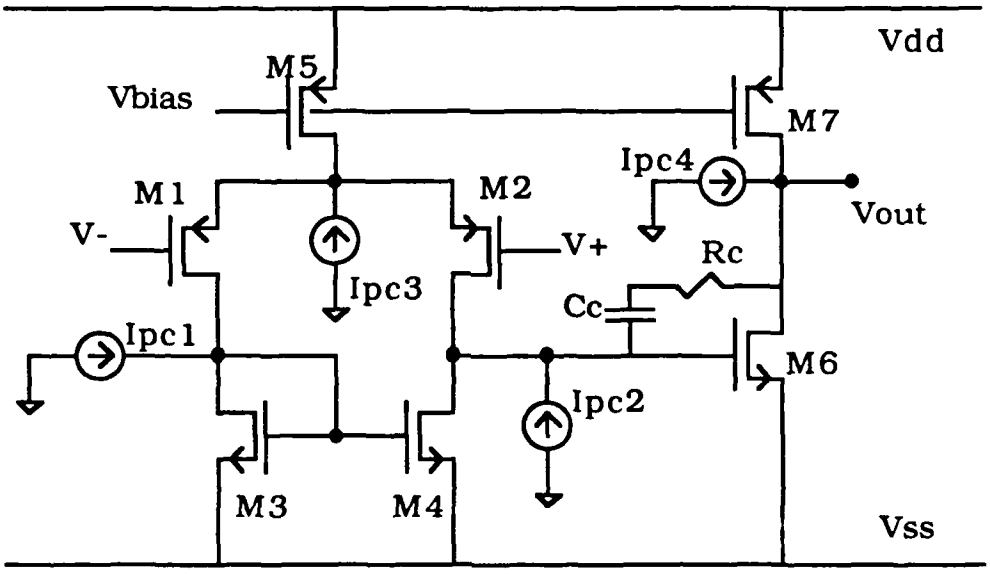

Figure 3.1: Two-stage operational amplifier with net photocurrent sources

Table 3.1: Typical photocurrent source levels per radiation dose rate for the two-stage operational amplifier

Photocurrent source	Current level (nA/megarad/sec)
Ipc1	40.0
Ipc2	25.0
Ipc3	60.0
Ipc4	90.0

dose rate for an SOI technology. For this and all remaining simulations, a +/- 20% photocurrent matching uncertainty is assumed with the sign of the net photocurrent selected to maximize the operational amplifier response. For each radiation level simulated, an input-referred DC voltage value is generated as listed in Table 3.2. Notice that the input-referred offset varies almost linearly up to 0.24 volts at a simulated radiation dose level of $1 \cdot 10^{9}$ rads/sec. At a dose rate of $1 \cdot 10^{10}$ rads/sec, the operational amplifier can no longer maintain stable operation use the net photocurrents overwhelm at least one amplifier node. These circuit simulations can be used to determine the input-referred offset versus radiation dose rate for a given operational amplifier and the critical dose rate at which the circuit begins to completely malfunction.

The steady-state analysis method may be modified slightly to identify sensitive nodes. By applying current to each node separately and monitoring the input-referred offset, the sensitivity of each node may be characterized. Improvements to the circuit, such as by photocurrent matching, may then be considered for these sensitive nodes. Table 3.3 lists the relative input-referred responses with $1.0 \cdot 10^{-9}$A currents applied to each node. Notice that the nodes with the highest sensitivity per applied current are at the drains of the input pair.

Table 3.2: Simulated input-referred offset voltages for various dose rates

Dose rate (rads/sec)	Input referred voltage (V)
1E5	4.9E-5
1E6	5.3E-4
1E7	5.2E-3
1E8	4.6E-2
1E9	2.4E-1

Table 3.3: Input referred offset voltage with 10^{-9}A applied to each node tested separately

Photocurrent source	Relative offset (V/mA)
Ipc1	-36.740
Ipc2	27.550
Ipc3	-0.158
Ipc4	0.056

The input-referred offsets for each node in steady-state analysis may be estimated using simple calculations. The net photocurrent at a node is compensated for by a shift in the input voltage which produces an equal but opposite current at the given node. For example, consider again the operational amplifier in Figure 3.1 and assume all photocurrent sources are off except the source at the output. The net transconductance from the input to the output node may be calculated to determine the estimated input-referred offset needed to compensate for a net photocurrent at the output node. To determine the transconductance, G, from the input to the output node, multiply the voltage gain from the amplifier input to the gate of the second-stage driver times the transconductance of the second-stage driver. Using simulated parameter values

gm2 = 27.1 micromhos

gm6 = 171.0 micromhos

gd2 = 0.104 micromhos

gd4 = 0.155 micromhos

yields

$$G = [gm2 / (gd2 + gd4)] * gm6$$

$$= [27.1 \cdot 10^{-6} / (0.104 \cdot 10^{-6} + 0.155 \cdot 10^{-6})] * 171.0 \cdot 10^{-6}$$

$$G = 0.0179 \text{ Amps/Volt}$$

Therefore G is the magnitude of the compensating current at

the output node per volt of input-referred offset voltage. This value is consistent with the relative input-referred offset voltage listed in Table 3.3. Likewise, hand calculations may be used to estimate values for other node sensitivities.

Often for steady-state analysis, two symmetric nodes may compensate for each other. Consider the symmetric nodes at the drains of M1 and M2 in Figure 3.1. As shown in Table 3.3, these nodes have input-referred offsets of approximately equal magnitudes but of opposite sign. Therefore by superposition, the combined input-referred offset contribution of these nodes may be minimized if the photocurrent response of each node is nearly equal. However, net photocurrent levels that approach the magnitude of the quiescent operating currents may significantly debias the circuit and cause a malfunction.

3.4 TRANSIENT ANALYSIS

Transient analysis simulates the type of radiation that occurs over very short periods of time such as those expected during a nuclear detonation. The response of the operational amplifier to transient radiation is dependent upon the photocurrent magnitude, photocurrent sensitivity of each node and the operational amplifier configuration as in the case of steady-state analysis. In addition, the location of each node relative to the signal path is an

important consideration in transient analysis.

Typically, the transient radiation response for a circuit is determined using a flash X-ray radiation chamber as a test source. Frequently, transient radiation simulations are performed to simulate flash X-ray photocurrents instead of the wide variety of possible radiation responses due to nuclear detonations. To be consistent with this practice, all transient radiation simulations in this paper use a pulse width of 50 nanoseconds unless otherwise indicated.

The two-stage operational amplifier in Figure 3.1 is used to demonstrate the transient analysis method. The net photocurrents used are those listed in Table 3.1 for a dose rate of $1 \cdot 10^{8}$ rads/sec except that the net photocurrents are pulsed on for only 50 nanoseconds. The simulated operational amplifier output responses for gain configurations of 1X, 10X and 100X are shown in Figure 3.2. Note the simulated output response for the 10X and 100X gain configurations have approximately the same peak response. The 1X gain configuration has a lower peak response due to the faster closed-loop response of the amplifier. The slower closed-loop response time for higher value gain configurations causes the recovery times to roughly scale linearly with the gain configuration.

Net photocurrents applied to circuit nodes yield perturbations in the normal nodal voltages, which may then

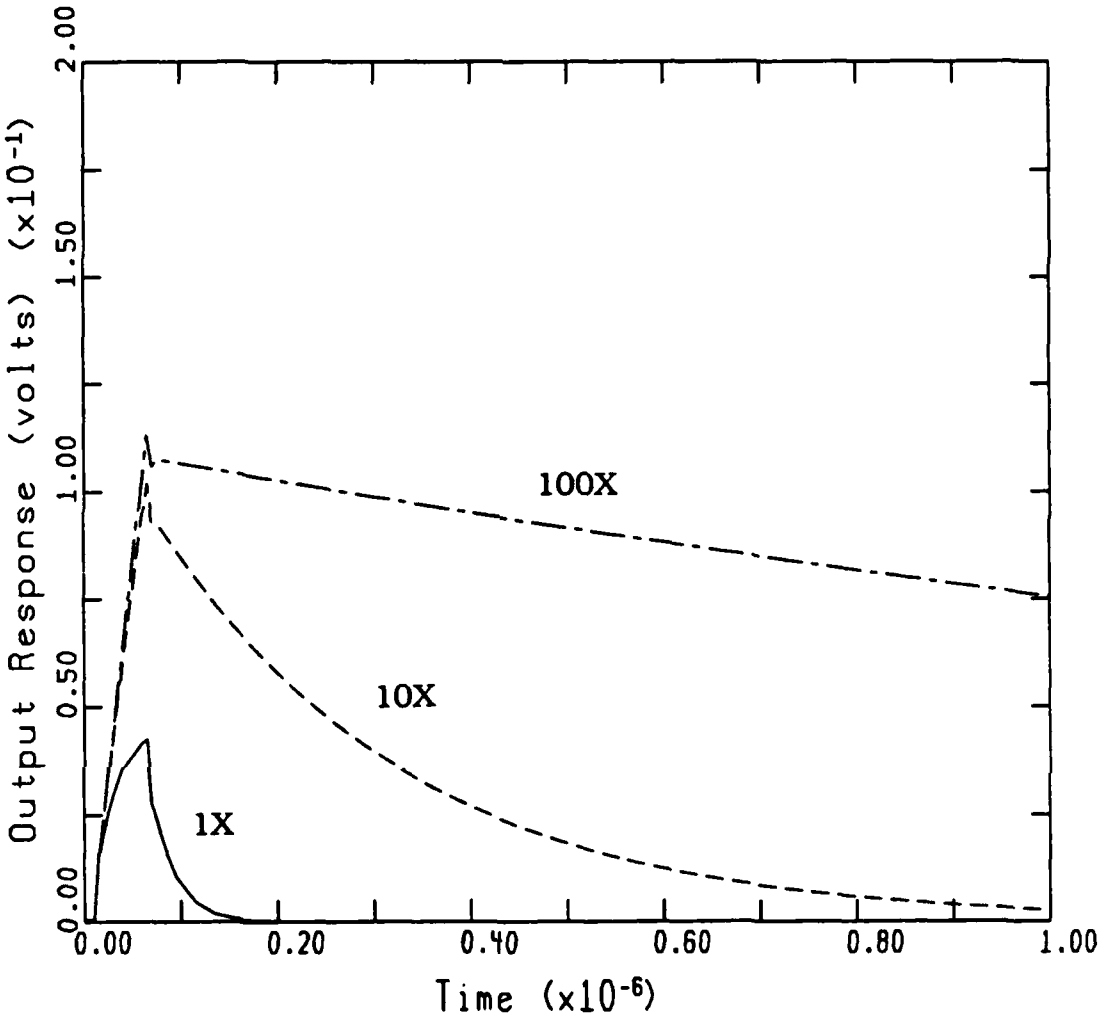

Figure 3.2: Simulated operational amplifier transient photocurrent responses

be amplified at the output. These perturbations are generally too short to allow time for the closed-loop response of the amplifier feedback to compensate for the transient. Instead, each perturbation along the signal path will cause its own signature at the output relative to the perturbation at each node. Moreover, these individual responses interact to produce a complex composite response. This suggests that the best method for attempting to reduce the operational amplifier transient photocurrent response is to minimize the net photocurrent at each node.

Transient photocurrent response simulations may be very sensitive to the accuracy to the capacitance parameters used in the simulator's models used. The initial voltage response at each node may be approximated by the following equation.

$$\Delta V = C_T \times I_P \times W_P$$

Where C_T is the total capacitance at the node, I_P is the net photocurrent applied to the node, and W_P is the duration of the photocurrent pulse. If the capacitance modeling at each node is incorrect, there will be errors in the simulated output response.

As in the steady-state case, hand calculations are useful for determining nodes sensitive to transient radiation. The transient photocurrent sensitivity of a node may be estimated by calculating the capacitance of the node and

by calculating the gain of the operational amplifier between that node and the output. For example, consider the drain of M2 in Figure 3.1, which typically has a small capacitance. The voltage gain from this node to the output is considerable due to the voltage gain of M6. Therefore, its transient photocurrent sensitivity is large compared to, for example, the transient photocurrent sensitivity of the output node which has no voltage gain and may also have a relatively large capacitance. This implies that reducing the net photocurrent at the drain of M2 may significantly improve the simulated transient radiation response of the operational amplifier.

Operational amplifier symmetries are useful for photocurrent compensation of steady-state radiation environments but have limited use in transient radiation environments. Consider again the differential pair of the two-stage operational amplifier in Figure 3.1. In the steady-state case, the overall response of the amplifier may improve if Ipc1 approximately equals Ipc2. In contrast, precise cancellations at these nodes will not occur for transient environments. Instead, the finite delay required for the photocurrent response of Ipc1 to propagate through the current mirror to the drain of M2 may cause the response of Ipc1 to arrive too late to compensate for the response of Ipc2.

CHAPTER 4: RADIATION HARDENING STRATEGIES

4.1 TOPOLOGY SELECTION

Topology selection is one of the most important steps in developing radiation hardened operational amplifiers. Usually a standard topology is initially selected based on the circuit application. Then the radiation response characteristics of the circuit are studied to determine if the circuit will fulfill the requirements for radiation hardness. Finally, the circuit topology may be modified and re-examined if necessary.

The operational amplifier topology characteristics desired are dependent upon the technology to be used. As indicated in Chapter 2, the strategy needed to reduce the net photocurrent response at each circuit node is dependent upon the technology used. For bulk CMOS, complementary transistors must be present to achieve photocurrent compensation at sensitive nodes. For SOI CMOS, transistors along a rail-to-rail current path must be selected to have approximately equal photocurrents from drain to source to ensure that little net photocurrent is generated at each node.

Often topologies that are useful for one technology may not be useful for the other. One example is an output source follower subcircuit as shown in Figure 4.1 using n-channel transistors. If the subcircuit is to be implemented in an SOI process, the collection volumes of M1 and M2 may be scaled to ensure that the photocurrents entering and leaving the output node are matched. Conversely for bulk CMOS, the photocurrent generated at the output node for each transistor is in the same direction and therefore compensation is not possible for this subcircuit. In general, SOI CMOS radiation hardened topologies are easier to develop than bulk CMOS technologies because SOI CMOS operational amplifiers do not require complementary devices for compensation.

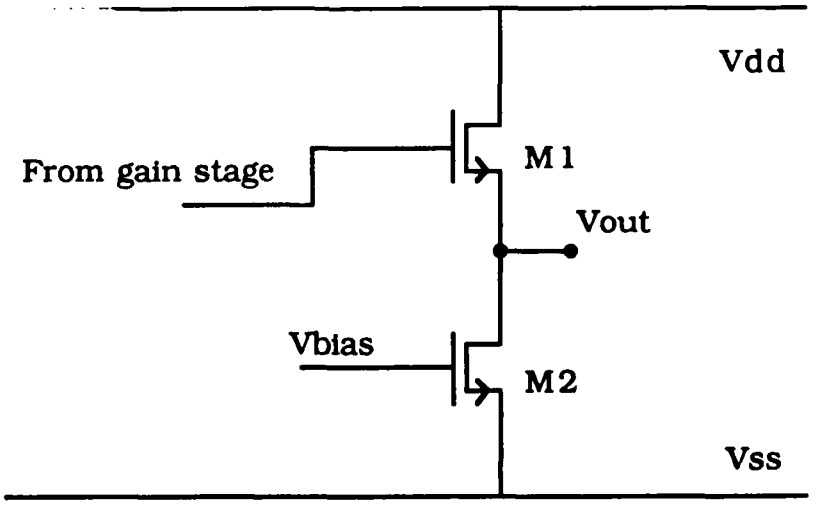

Figure 4.1: N-channel source follower output subcircuit

4.2 CURRENT DENSITY

Increasing current density is another strategy that may be used for radiation hardened operational amplifiers since the photocurrents generated are approximately proportional to the sizes of the devices used. The general trend toward higher circuit density with smaller device geometries tends to reduce photocurrent collection volumes. To maintain the same power dissipation through each device while decreasing the device collection volumes, the W and L values for each device may be scaled down proportionately to maintain the same W/L ratios. For constant W/L ratios in SOI CMOS, the photocurrent collection volumes are reduced in proportion to the product of the device dimensions. For bulk CMOS, the reduction in photocurrent collection volumes is limited by the carrier diffusion lengths.

Generally, the transistor output conductance is inversely proportional to the device channel length. For gain stages where the output resistance is determined by the transistor output conductances alone, the voltage gain is reduced in proportion to the reduction in channel length. Operational amplifier designs that utilize the shortest channel lengths are usually favored if the DC gain is not critical to the application.

Increasing the operating bias (Vgs-Vt) for certain devices may be used in conjunction with photocurrent volume

scaling strategies to enhance the current density. The width of a device may be scaled down by increasing Vgs-Vt since the device quiescent drain current is proportional to the W/L ratio and the square of Vgs-Vt. However, in many cases, an increase in Vgs-Vt may compromise the common-mode input range or output swing.

Higher power dissipation does not directly improve transient radiation response since the node voltage perturbations are primarily dependent upon the capacitance at the node. Increasing the power dissipation may be useful if a minimal recovery time is desired after a high intensity radiation transient. In this case, the higher quiescent currents minimize the time required for the operational amplifier to return to its normal quiescent bias voltages after the transient. Also, higher quiescent operating currents during steady-state radiation exposure can often aid in maintaining circuit operation. For systems with limited power supply capabilities, increasing power dissipation may be an unfavorable method for radiation hardening.

4.3 PHOTOCURRENT COMPENSATION

Effective photocurrent compensation may significantly improve the radiation hardness of an operational amplifier. In this section, basic compensation techniques will be discussed for bulk CMOS and SOI CMOS technologies. Then an

example is used to demonstrate a photocurrent compensation strategy for an SOI CMOS subcircuit.

Figure 4.2 shows a complementary pair of bulk CMOS devices with their drains connected to provide photocurrent compensation. The net photocurrent response at the drain connection of the devices will be minimized if the devices are fabricated so that Idb1 approximately equals Idw2. Often these photocurrents can be controlled by scaling the collection volumes of each device drain without affecting their W and L dimensions. Another option is to add a complementary junction to a node if necessary to achieve the photocurrent compensation needed.

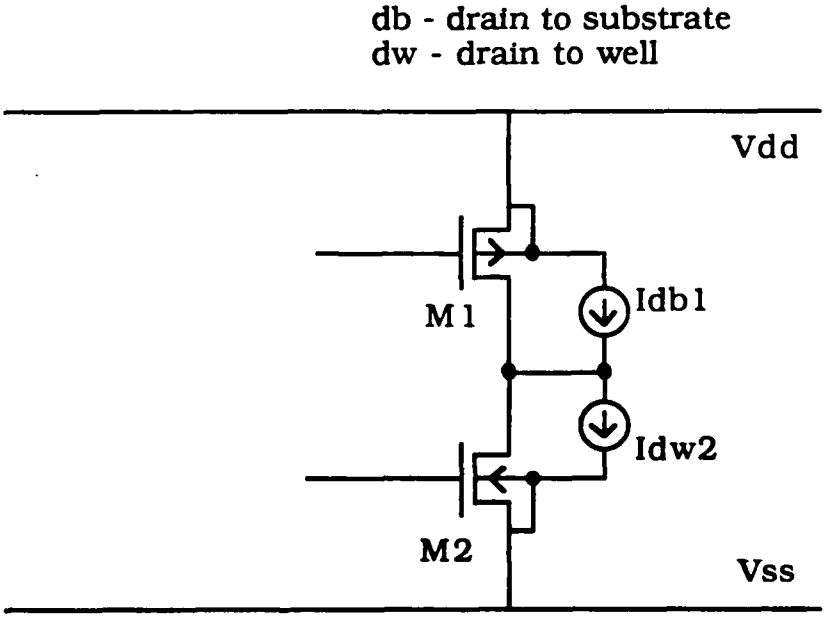

Figure 4.2: Series connected bulk CMOS transistors for photocurrent compensation

Photocurrent compensation for SOI CMOS may be performed on the series connected transistors shown in Figure 4.3. The net photocurrent at the drains of M1 and M2 may be minimized if collection volumes of M1 and M2 are scaled to ensure that the photocurrents generated are approximately equal. This figure shows only two devices in the rail-to-rail photocurrent path, but several devices in series may be compensated for by using the same strategy.

The differential amplifier stage in Figure 4.4 is used to demonstrate the transistor volume matching strategy for photocurrent compensation. The nodes at the drains of M1 and M2 are the most sensitive and therefore must be photocurrent compensated. Since M1 and M3 are symmetric with M2 and M4, respectively, only dimensions for M2 and M4

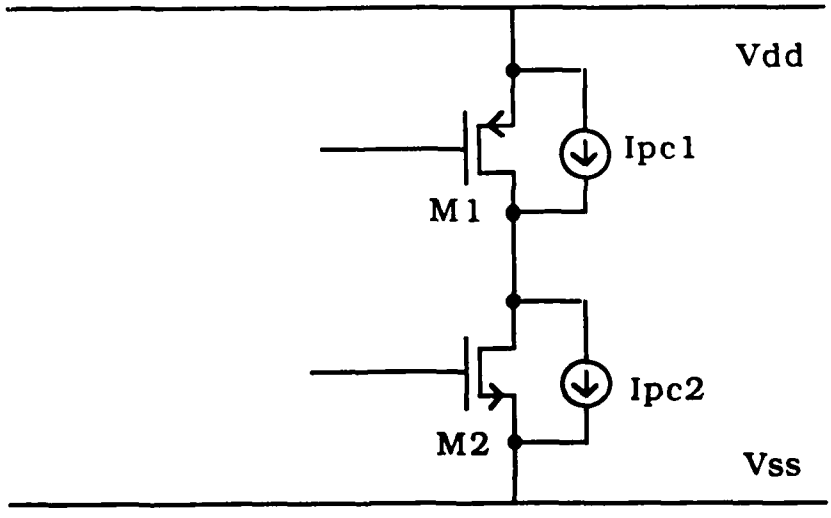

Figure 4.3: Series connected SOI CMOS transistors for photocurrent compensation

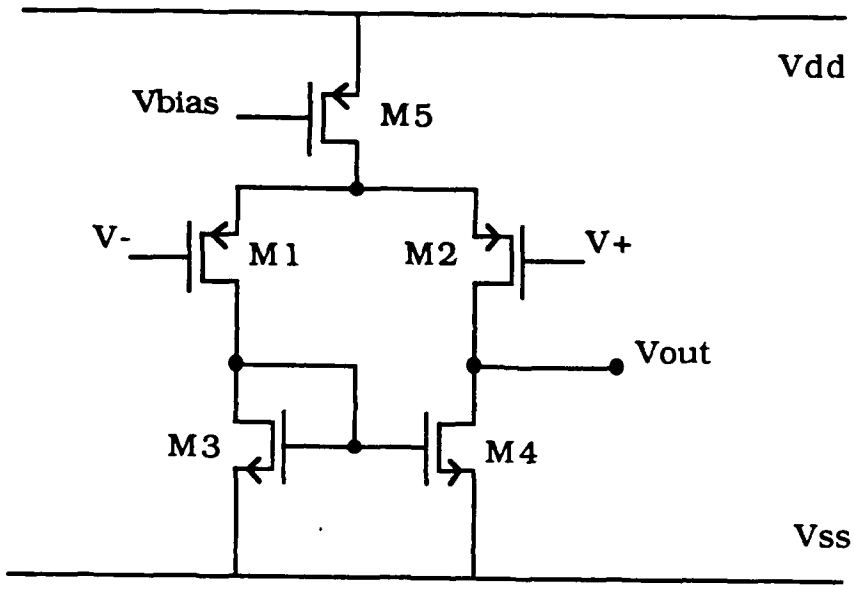

Figure 4.4: SOI CMOS differential amplifier

need to be calculated. As a design specification, assume the following:

W/L (M2) = 10 microns

W/L (M4) = 40 microns

min W = min L = 2 microns

To minimize the net photocurrent, the total device areas (W times L) must be equal and the total device volumes (or areas) minimized. The following W and L values are found:

W (M4) = 80 microns

L (M4) = 2 microns

W times L (M4) = 160 square microns

W (M2) = 40 microns

L (M2) = 4 microns

W times L (M2) = 160 square microns

Notice that the width and length of M4 are twice their minimum possible values in order to maintain the volume matching.

4.4 OVERCOMPENSATION/UNDERCOMPENSATION

Since exact photocurrent matching is difficult, a direction of net photocurrent response may be preferred to achieve a less radiation sensitive design. A deliberate mismatch can be used to ensure that the sign of net photocurrent response will cause an increase in the quiescent current rather than a decrease. This will generally help to maintain circuit functionality through a radiation transient provided additional supply current is available. The magnitude of the the intentional compensation mismatch must be at least as large as the photocurrent matching errors expected.

This strategy is particularly important for bias circuits which should be designed to ensure that the amplifier bias current sources tend to increase during a radiation transient. As an example, a diode-connected SOI CMOS bias circuit is shown in Figure 4.5 which has a bias voltage output suitable for top rail connected current sources. If the area of M2 is greater than the area of M1, the bias voltage will decrease during a radiation transient which will enhance the quiescent currents in the operational amplifier. To select values for W and L for M1 and

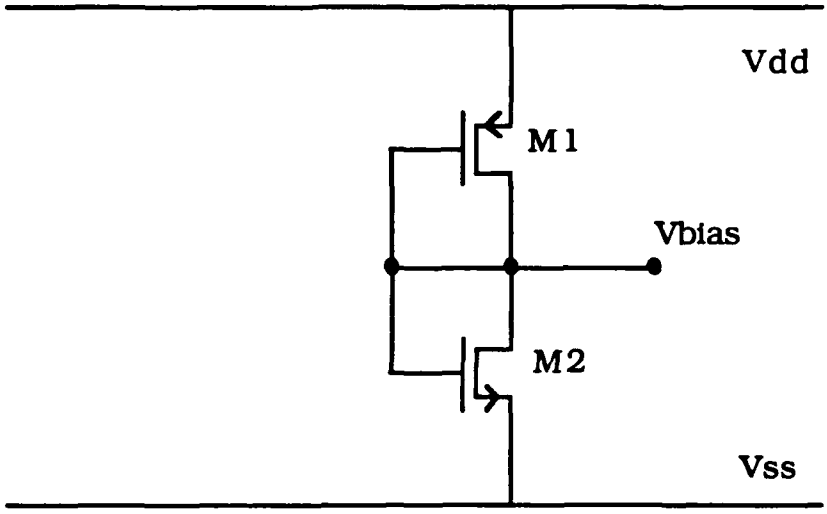

Figure 4.5: Diode connected bias circuit

M2, assume the specifications as follows:

W/L (M1) = 40 microns

W/L (M2) = 5 microns

min W = 2 microns

min L = 2 microns

Assume a possible photocurrent matching error of +/-20% and select the W and L values for minimum device areas. Setting the compensation mismatch equal to the photocurrent

matching error, the results are as follows:

W (M1) = 80 microns

L (M1) = 2 microns

W times L = 160 square microns

W (M2) = 31 microns

L (M2) = 6.2 microns

W times L = 192 square microns = 1.2 x 160

The W and L values for M2 have been approximately tripled to achieve a 20% compensation mismatch between M1 and M2.

CHAPTER 5: IMPLEMENTATION OF RADIATION HARDENED OPERATIONAL AMPLIFIERS

5.1 INTRODUCTION

This chapter will discuss two specific implementations of operational amplifiers in an SOI CMOS technology. First, the technology used will be described. Then details relating to the design issues for a folded-cascode and a three-stage operational amplifier and their bias circuits are discussed using the methods introduced in the previous chapters. The chapter concludes with simulated photocurrent responses for each radiation hardened design.

5.2 DESCRIPTION OF TECHNOLOGY

The SOI CMOS technology used for the operational amplifiers described here is the SIMOX (SIlicon with IMplanted buried OXide) process developed by Texas Instruments, Incorporated for the Defense Nuclear Agency [4]. This 1.2 micron technology has a body-tied-to-source fabrication capability and utilizes one polysilicon and two metal layers. Parasitic capacitances between metal layers are used to fabricate on-chip capacitors.

The body-tied-to-source configuration is selected throughout since the floating-body configuration leads to excess radiation-induced photocurrents through the photocurrent multiplier effect. In addition, the body-to-source connection also eliminates the kink effect which increases transistor output conductance and degrades the gain of each amplifier gain stage.

All photocurrent response calculations in this chapter assume that the transistor body is fully depleted of carriers and that there is photocurrent collection from the total active volume of each transistor. This approximation greatly simplifies the photocurrent estimation calculations during the circuit design process and does not require the use of photocurrent data.

5.3 TOPOLOGY

5.3.1 FOLDED-CASCODE

A standard topology for a folded-cascode operational amplifier is shown in Figure 5.1. This type of operational amplifier is primarily used for driving capacitive loads for on-chip applications. Some initial observations may be made about radiation hardening of this operational amplifier. First, there are rail-to-rail photocurrent paths by which every photocurrent generated in the circuit may be compensated. Also, there are four split rail-to-rail photo-

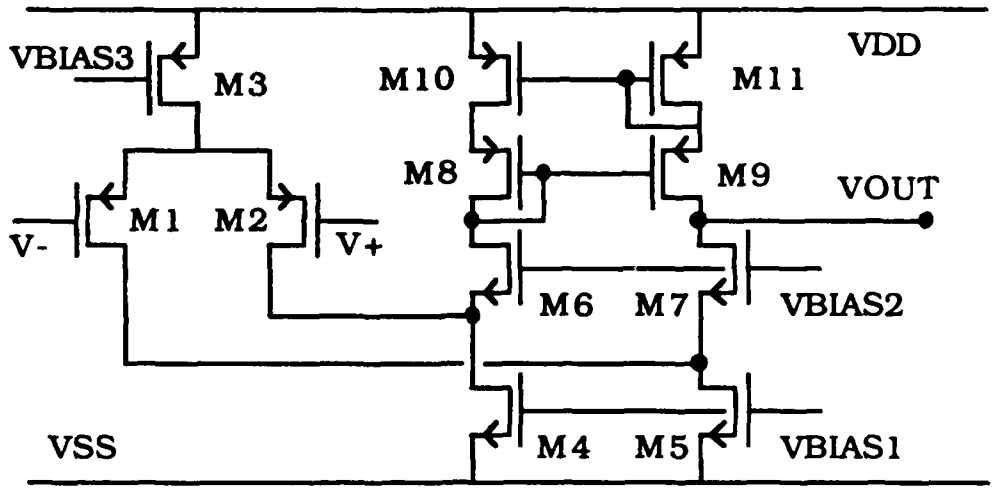

Figure 5.1: Folded cascode operational amplifier topology

current paths which require photocurrent compensation. Four paths from the Vdd rail to the Vss rail can be found as follows:

PATH #1 - M3 through M1 to M5

PATH #2 - M3 through M2 to M4

PATH #3 - M10 through M8 through M6 to M4

PATH #4 - M11 through M9 through M7 to M5

M3, M4 and M5 each share two photocurrent paths and therefore each must be considered twice when selecting device volumes.

Table 5.1 lists the widths and lengths used in the folded-cascode operational amplifier of Figure 5.1. The circuit is designed to drive a 5 picofarad load with a unity-gain frequency of 6.3 megahertz. The gain is 66 dB and its quiescent power dissipation is 1.0 milliwatt. The W

Table 5.1: Transistor sizes for the folded cascode operational amplifier

Transistor	W (um)	L (um)	W/L
M1	40	1.2	33.3
M2	40	1.2	33.3
M3	40	2.4	16.7
M4	40	2.4	16.7
M5	40	2.4	16.7
M6	20	2.4	8.3
M7	20	2.4	8.3
M8	40	1.2	33.3
M9	40	1.2	33.3
M10	40	1.2	33.3
M11	40	1.2	33.3

and L values for M6 through M11 are selected to generate equivalent photocurrents through each device. The W and L values for M1, M2 and M3 are designed so that M3 generates the sum of photocurrents of M1 and M2. W and L values for M4 and M5 are designed to match photocurrents from the sum of photocurrents from M2 and M6 and M1 and M7, respectively.

5.3.2 THREE-STAGE

A three-stage operational amplifier with a push-pull output stage is shown in Figure 5.2. All devices have dc paths for photocurrent compensation with the exception of M15 which acts as a compensation resistor to remove the right half plane zero around transistor M6. Photocurrent from M15 will collect without compensation at the gate of

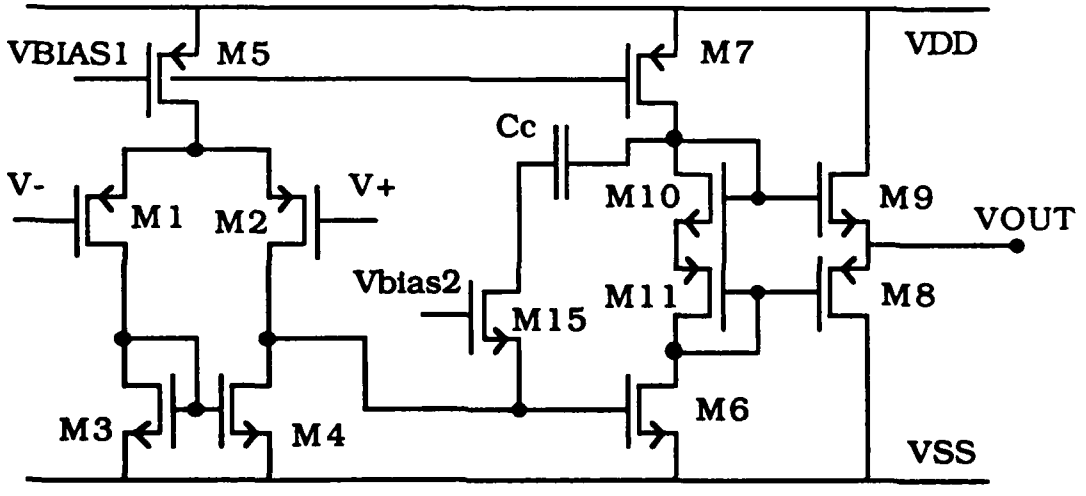

Figure 5.2: Three-stage operational amplifier with compensation resistor (M15)

M6. Since this is a highly sensitive node, the uncompensated photocurrent from M15 would dominate the overall transient radiation response.

An alternative means of right-half-plane zero compensation is to provide a source follower capacitor feedback path. This design, shown in Figure 5.3, includes a dc rail-to-rail current path through M15 and M16 so that photocurrent compensation is possible. The primary disadvantage is that it requires a quiescent current through M15 and M16 which increases the power dissipation of the circuit.

Table 5.2 lists the widths and lengths used in the three-stage operational amplifier of Figure 5.3. This circuit is designed to drive 600 ohms with an output swing of +/- 2.25 volts and a unity-gain frequency of 5.0

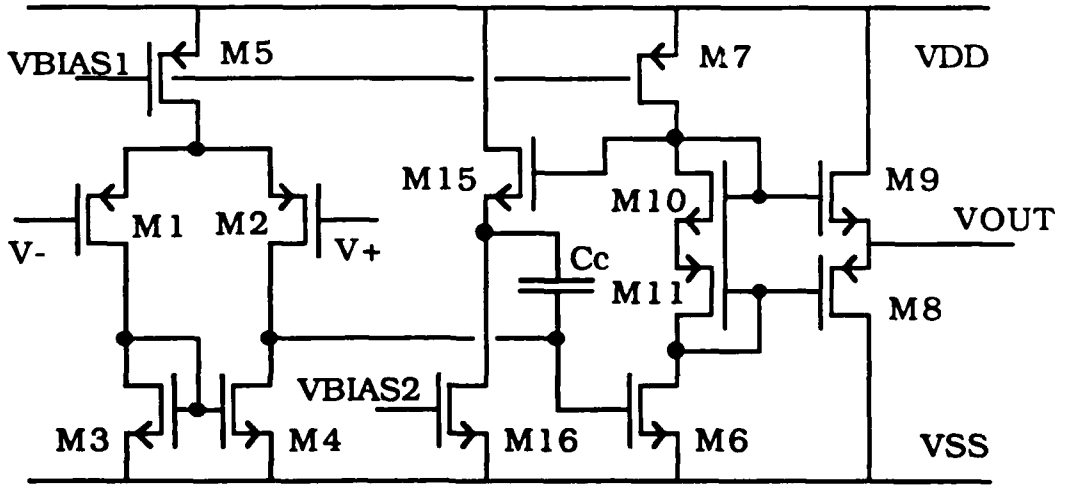

Figure 5.3: Three-stage operational amplifier with source follower compensation feedback

Table 5.2: Transistor sizes for the three-stage operational amplifier

Transistor	W (um)	L (um)	W/L
M1	5.0	2.4	2.1
M2	5.0	2.4	2.1
M3	5.0	2.4	2.1
M4	5.0	2.4	2.1
M5	20.0	1.2	16.7
M6	40.0	2.4	16.7
M7	40.0	2.4	16.7
M8	160.0	1.2	133.3
M9	160.0	1.2	133.3
M10	30.0	1.8	16.7
M10A	18.0	2.4	7.5
M11	30.0	1.8	16.7
M11A	18.0	2.4	7.5
M15	20.0	1.2	16.7
M16	20.0	1.2	16.7

megahertz. The quiescent power dissipation is 1.2 milliwatt. The W and L values for M1 and M3 and M2 and M4 are selected for matched photocurrents. The volume of M5 is selected to match the sum of the volumes of M1 and M2. Likewise, M8 matches M9, M6 matches M7, M10 matches M11, and M15 matches M16. M10 and M11 are designed to provide a slightly greater photocurrent response than M6 and M7 to ensure that the bias to M8 and M9 will not decrease during a radiation transient.

5.4 BIAS CIRCUITRY

Figure 5.4 shows a bias circuit that uses diode-connected p-channel and n-channel transistors. It has a rail-to-rail photocurrent path through all devices making it a desirable circuit type for radiation hardening strategies. Notice that the diode-connected configuration provides very little power supply rejection due to the supply voltage dependence of the current through the devices.

An alternative bias circuit topology using a depletion p-channel device is shown in Figure 5.5. It has considerably better power supply rejection than the previous design and maintains the advantages of a single rail-to-rail photocurrent path. However, this approach requires an additional mask step for the depletion implant.

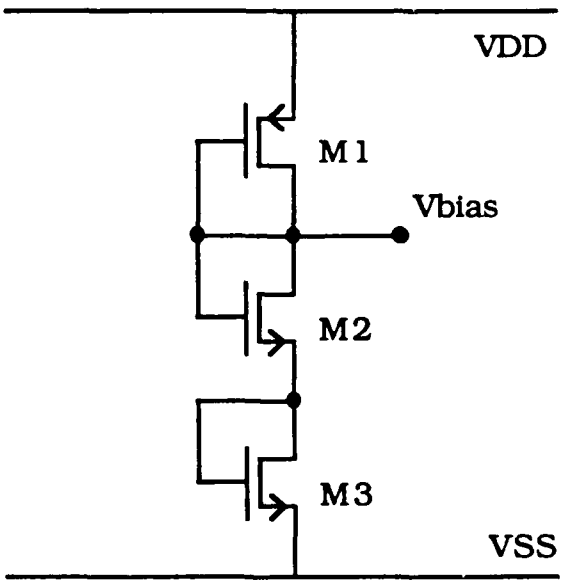

Figure 5.4: Bias circuit using diode connected transistors

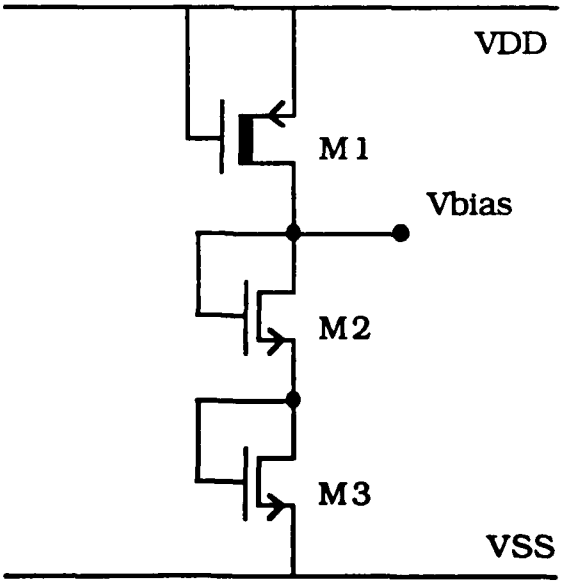

Figure 5.5: Bias circuit using a depletion transistor

Figure 5.6 shows a bias circuit using a Widlar current mirror which also provide good power supply rejection. It contains two rail-to-rail photocurrent paths, assuming that the resistor is implemented as a MOSFET channel. However, this circuit is particularly sensitive to net photocurrents at any off-rail node making it undesirable for radiation environments.

Another method for developing bias voltages is to use a standard voltage reference. Figure 5.7 shows a bias circuit that utilizes such a reference while still maintaining a rail-to-rail photocurrent path. This configuration is particularly suitable for applications where a single highly stable voltage supply may be used as a reference for multiple bias circuits.

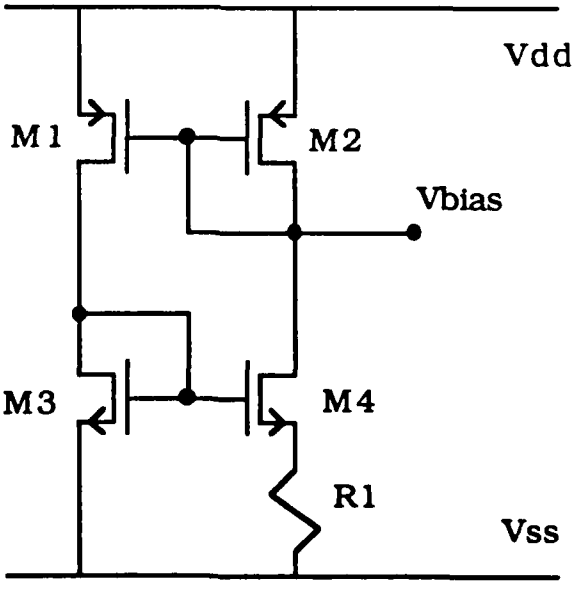

Figure 5.6: Widlar current mirror bias circuit

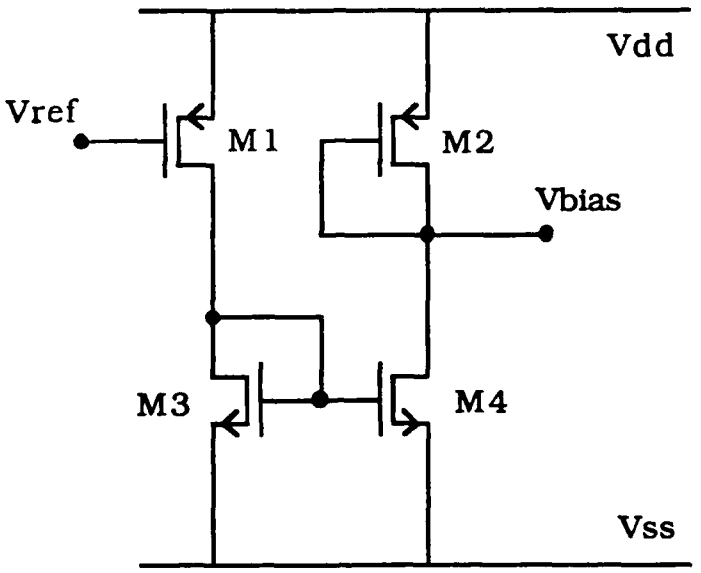

Figure 5.7: Bias circuit using an external voltage reference

5.4.1 FOLDED-CASCODE BIAS CIRCUIT

The bias circuit in Figure 5.8 is used for the folded-cascode operational amplifier on the test chip. The W, L and W/L values are listed in Table 5.3. Five diode-connected transistors are used to develop three bias voltages. It is designed for +/- 5 volt power supplies with a power dissipation of 0.2 milliwatt. Transistors M22, M23 and M24 are approximately 10% greater in area than M21 and M25 to ensure that each current source in the folded-cascode amplifier will have increased bias current during a radiation transient.

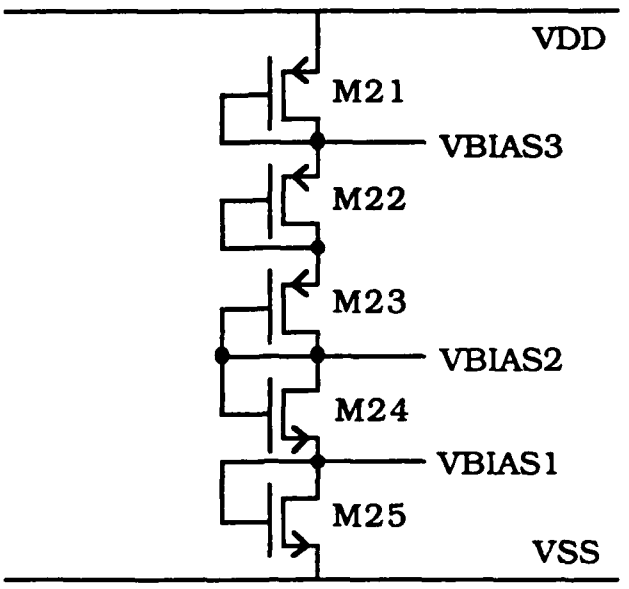

Figure 5.8: Bias circuitry for the folded cascode operational amplifier

Table 5.3: Transistor sizes for the folded cascode operational amplifier bias circuit

Transistor	W (um)	L (um)	W/L
M21	20.0	2.4	8.3
M22	6.6	8.4	0.8
M23	6.6	8.4	0.8
M24	14.0	3.6	3.9
M25	20.0	2.4	8.3

5.4.2 THREE-STAGE BIAS CIRCUIT

The bias circuit in Figure 5.9 is used in the three-stage operational amplifier and has W, L and W/L values as listed in Table 5.4. Five diode-connected transistors are used to generate two bias voltages. It dissipates 0.1 milliwatt with +/- 5 volt power supplies. Transistors M21 and M25 have matched photocurrents, and transistors M22, M23 and M24 are approximately 12% greater in area than M21 and M25 to ensure that the current sources in the three-stage operational amplifier have increased bias currents during a transient.

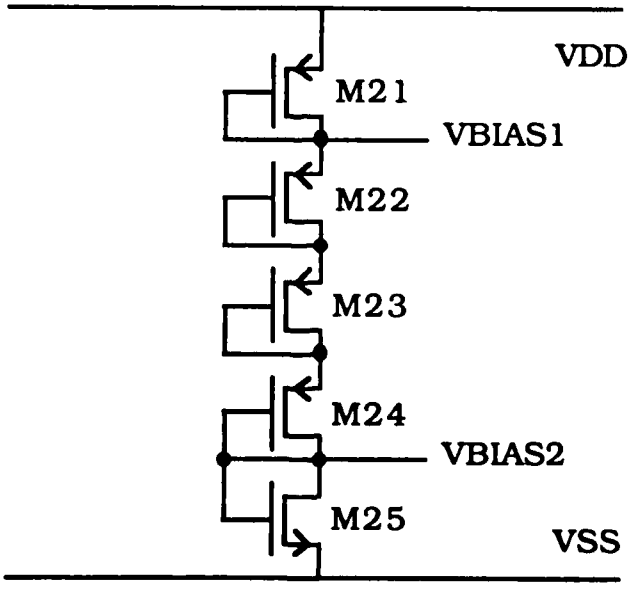

Figure 5.9: Bias circuitry for the three-stage operational amplifier

Table 5.4: Transistor sizes for the three-stage operational amplifier bias circuit

Transistor	W (um)	L (um)	W/L
M21	40.0	2.4	16.7
M22	7.2	15.0	0.5
M23	7.2	15.0	0.5
M24	7.2	15.0	0.5
M25	30.0	3.0	10.0

5.5 RADIATION PHOTOCURRENT SIMULATION DATA

Simulated transient radiation responses were generated for the folded-cascode and three-stage operational amplifiers. All simulations are performed for a transient radiation dose rate of $1 \cdot 10^{10}$ rads/sec. All net photocurrents at each node are applied using a DC pulse that simulates a 50 nanosecond radiation pulse occurrence. The net photocurrent simulated is chosen as discussed in Chapter 3.

5.5.1 FOLDED-CASCODE AMPLIFIER RESPONSE

The experimental folded-cascode operational amplifier and bias circuit designs of Figures 5.1 and 5.8 were simulated for transient radiation response. For these

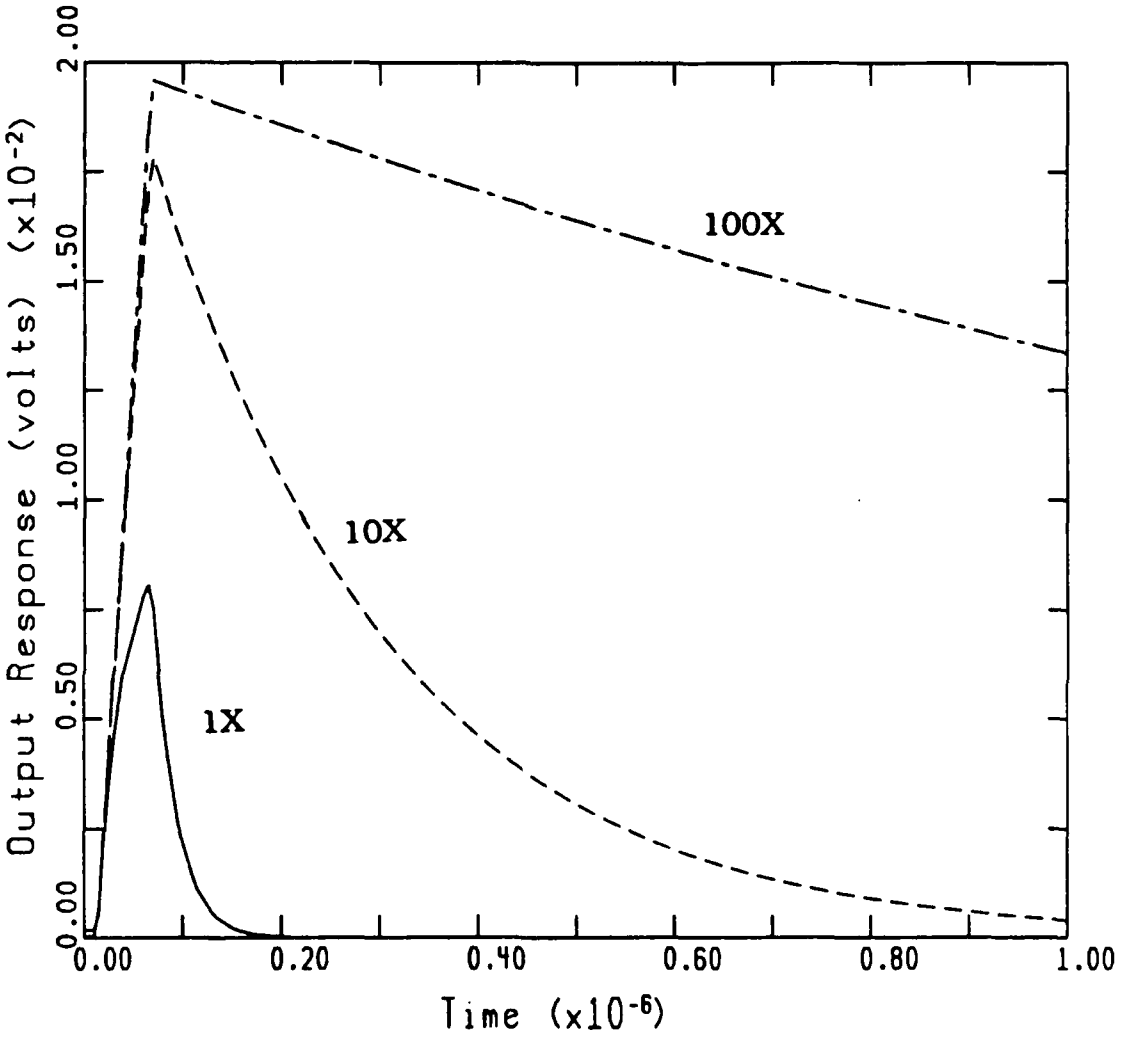

Figure 5.10: Simulated transient radiation output responses for the folded-cascode operational amplifier

simulations, the amplifier was connected in 1X, 10X and 100X non-inverting gain configurations with a 5 picofarad capacitor loading the output. The simulated transient radiation responses of Figure 5.10 show less than 20 millivolts of peak response.

5.5.2 THREE-STAGE AMPLIFIER RESPONSE

The experimental three-stage operational amplifier and bias circuit designs of Figures 5.3 and 5.9 were also simulated for transient radiation response. Again, the amplifier was connected in 1X, 10X and 100X non-inverting gain configurations but with a 600 ohm resistive output load. The simulated transient radiation output responses are shown in Figure 5.11. Again, the peak response in all cases remained below 20 millivolts, however, unlike the folded-cascode case, the gain of 1 case also shows a 7 millivolt negative excursion immediately following the photocurrent pulse. For both operational amplifiers, the recovery time tends to scale proportionately with the value of the closed-loop gain.

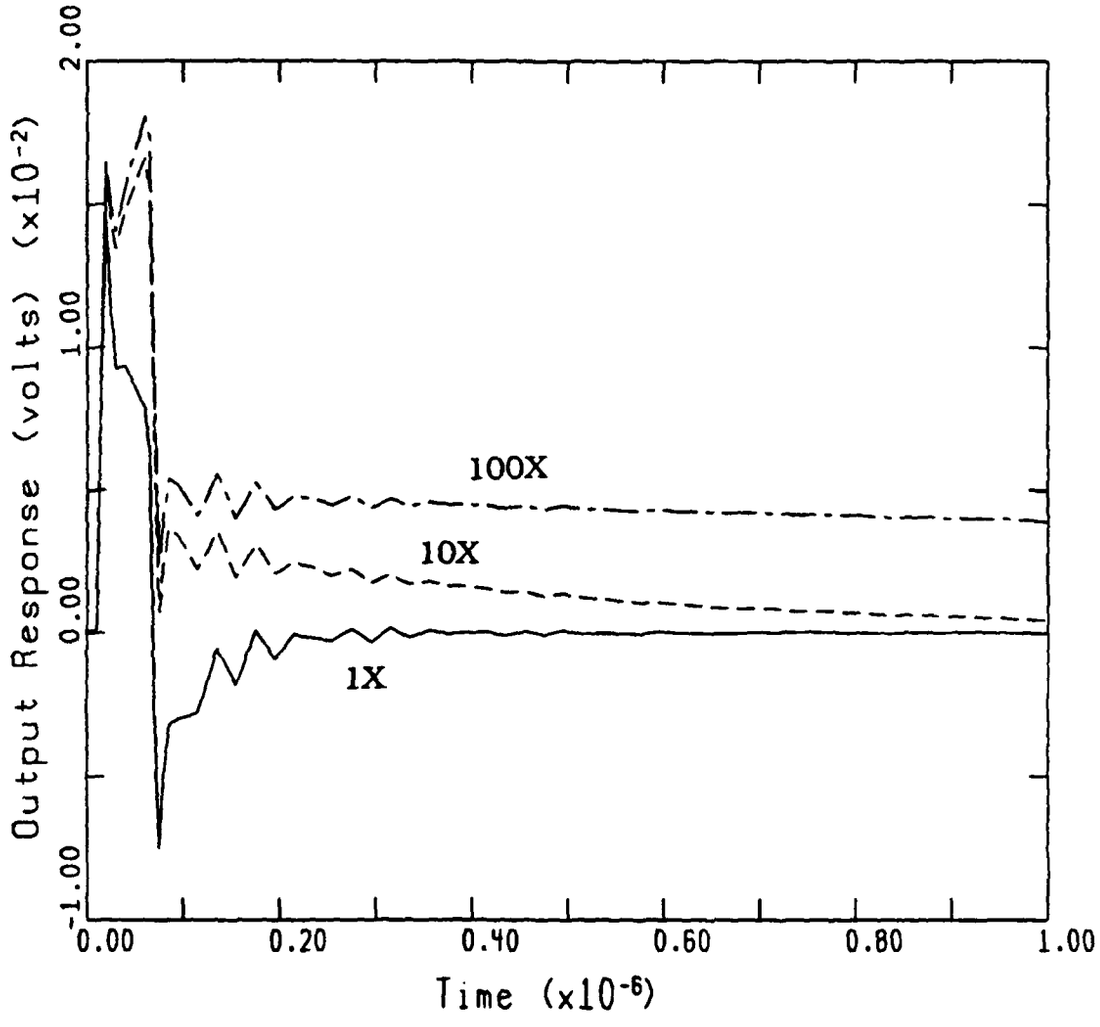

Figure 5.11: Simulated transient radiation output responses for the three-stage operational amplifier

CHAPTER 6: CONCLUSIONS

This thesis includes a number of strategies for radiation hardening of CMOS operational amplifiers in both bulk and SOI technologies. Heuristic approaches and simulations are used to select operational amplifiers for the desired applications. Many compromises between performance and radiation hardness are encountered. SOI CMOS is the preferred technology for high level radiation environments due to the significantly lower photocurrent responses and because the well defined photocurrent collection volumes produce more predictable photocurrent responses for photocurrent matching strategies at each node. Simulations have demonstrated that output responses of a few millivolts are possible with SOI technology operational amplifiers irradiated with a $1 \cdot 10^{10}$ rads/sec dose rate. These results are far superior to any previous work in bulk CMOS or dielectricly isolated bipolar technologies.

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